

## Description

The PSMTO100V120 uses split gate trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. This device is suitable for power management and high efficiency applications at high switching frequencies applications.

### MOSFET Product Summary

$V_{DS}(V)$	$R_{DS(on)}(m\Omega)$	$I_D(A)$
100	3.2@ $V_{GS} = 10V$	189

## Feature

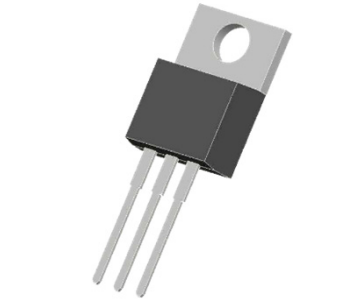
- Low  $R_{DS(ON)}$  - Ensures On-State Losses are Minimized
- Excellent  $Q_{gd} \times R_{DS(ON)}$  Product(FOM)
- Advanced Technology for DC-DC Converts
- Small Form Factor Thermally Efficient Package  
Enables Higher Density End Products
- 100% UIS (Avalanche) Rated
- Lead-Free Finish ; RoHS Compliant
- Halogen and Antimony Free. "Green" Device

## Applications

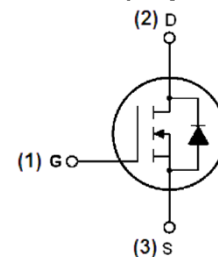
- PWM applications
- Load switch
- Power management
- DC-DC Converters
- Wireless Chargers

## Absolute maximum rating@25°C

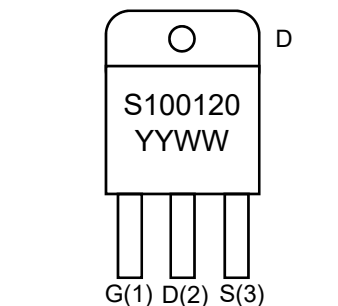
Rating	Symbol	Value	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous <sup>1)</sup>	$I_D$	$T_C=25^\circ C$	189
		$T_C=100^\circ C$	134
Pulsed Drain Current <sup>2)</sup>	$I_{DM}$	757	A
Single Pulse Avalanche Current @ L=0.1mH	$I_{AS}$	72	A
Single Pulse Avalanche Energy @ L=0.1mH	$E_{AS}$	259	mJ
Total Power Dissipation <sup>4)</sup>	$P_D$	$T_C=25^\circ C$	254
		$T_C=100^\circ C$	127
Thermal Resistance , Junction-to-Case <sup>4)</sup>	$R_{\theta JC}$	0.59	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>3)</sup>	$R_{\theta JA}$	32	$^\circ C/W$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ C$



**TO-220 (Top View)**



**Schematic diagram**



**Marking (Top View)**

## Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	
<b>Off Characteristics</b>							
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100V, V_{GS} = 0V$	$T_J = 25^\circ C$	-	-	1.0	$\mu A$
			$T_J = 55^\circ C$	-	-	10	
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	$\pm 100$	nA	
<b>On Characteristics<sup>5)</sup></b>							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	3.0	4.0	V	
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 20A$	-	3.2	3.8	m $\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 5V, I_D = 20A$	-	46	-	S	
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = 1A$	-	0.7	1.2	V	
<b>Dynamic Characteristics<sup>6)</sup></b>							
Input Capacitance	$C_{iss}$	$V_{DS} = 100V, V_{GS} = 0V, f = 1.0MHz$	-	4799	-	$\mu F$	
Output Capacitance	$C_{oss}$		-	1256	-		
Reverse Transfer Capacitance	$C_{rss}$		-	50	-		
<b>Switching Characteristics<sup>6)</sup></b>							
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 100V, V_{GS} = 10V, I_D = 20A, R_{GEN} = 3\Omega$	-	10	-	ns	
Turn-on Rise Time	$t_r$		-	17	-		
Turn-Off Delay Time	$t_{d(off)}$		-	44	-		
Turn-Off Fall Time	$t_f$		-	23	-		
Total Gate Charge @ $V_{GS} = 10V$	$Q_g$	$V_{DS} = 100V, I_D = 20A, V_{GS} = 10V$	-	68	-	nC	
Total Gate Charge @ $V_{GS} = 6V$			-	44	-		
Gate-Source Charge			$Q_{gs}$	-	19		-
Gate-Drain Charge			$Q_{gd}$	-	15		-
Gate Resistance	$R_g$	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$	-	1.5	-	$\Omega$	
<b>Drain-Source Diode Characteristics</b>							
Reverse Recovery Time	$t_{rr}$	$I_F = 20A, di/dt = 100A/\mu s$	-	62	-	ns	
Reverse Recovery Charge	$Q_{rr}$		-	130	-	nC	
Diode Forward Current	$I_S$	-	-	-	189	A	

## Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test : Pulse width  $\leq 100\mu s$ , duty cycle  $\leq 2\%$ .
3. Device mounted on 1 inch FR4 PCB with 2oz.Copper.
4. Device mounted on infinite heatsink.
5. Measured under pulsed conditions. Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
6. Guaranteed by design, not subject to production.

Typical Characteristics

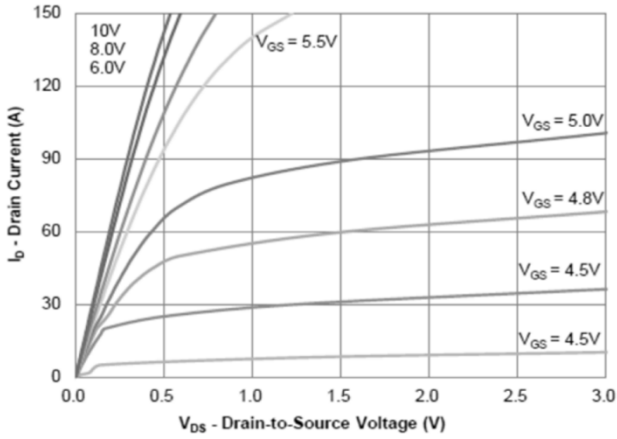


Figure 1: Output Characteristics

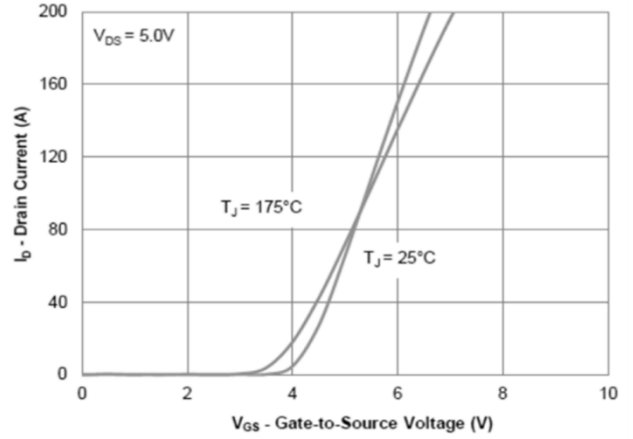


Figure 2: Transfer Characteristics

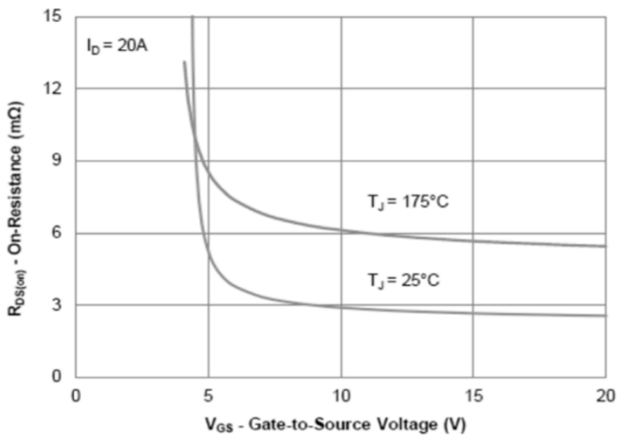


Figure 3: On-Resistance vs. Gate-Source Voltage

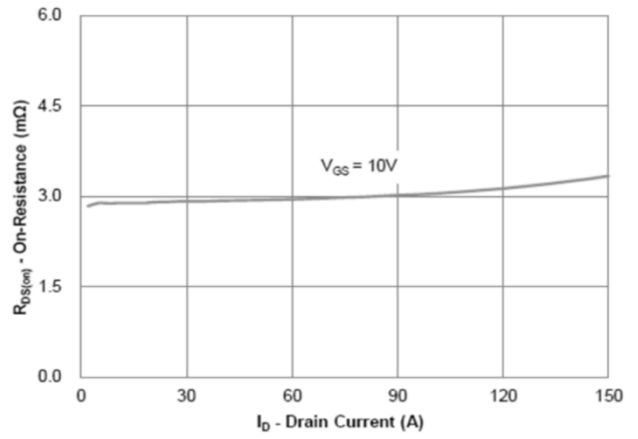


Figure 4: On-Resistance vs. Drain Current

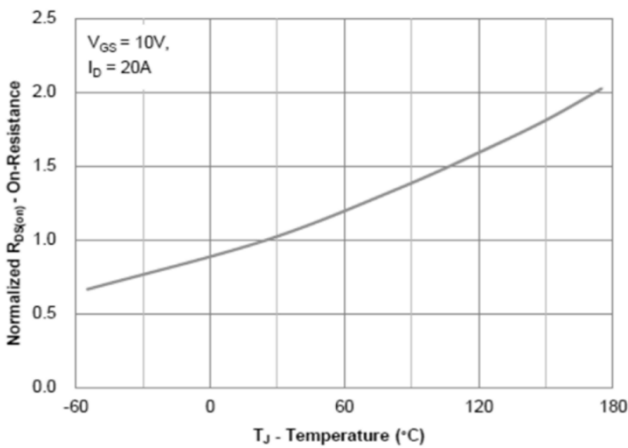


Figure 5: On-Resistance vs. Junction Temperature

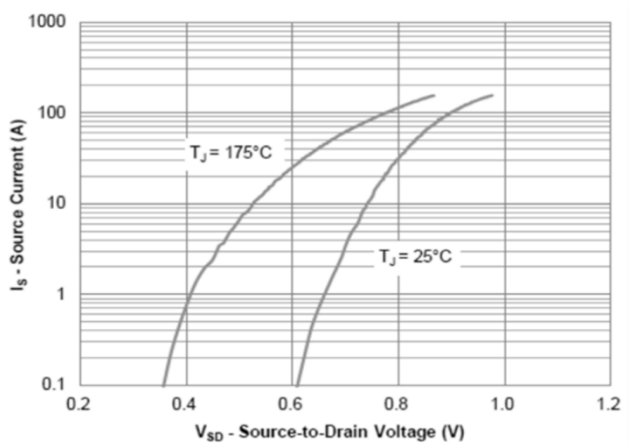


Figure 6: Source-Drain Diode Forward Voltage

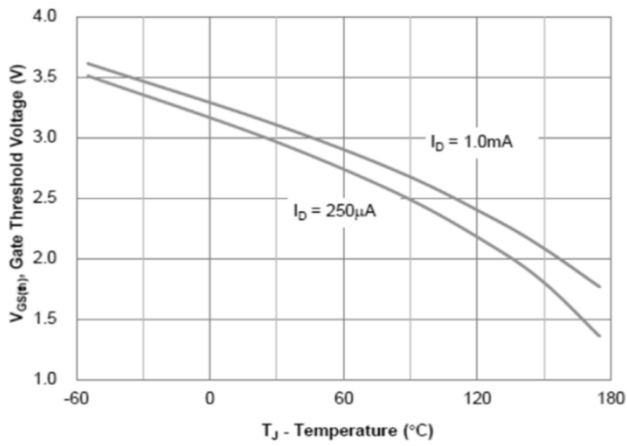


Figure 7: Gate Threshold Variation vs. Junction Temperature

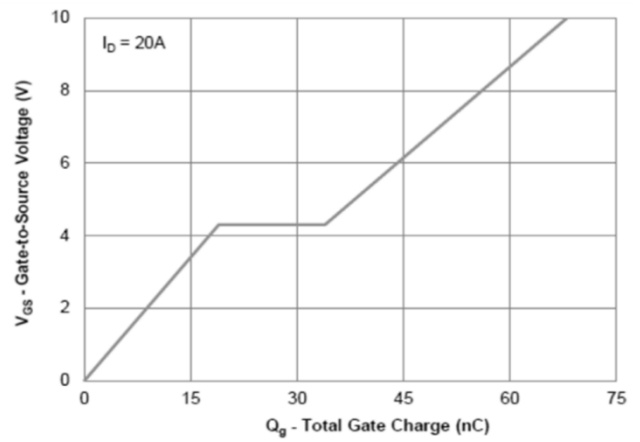


Figure 8: Gate Charge Characteristics

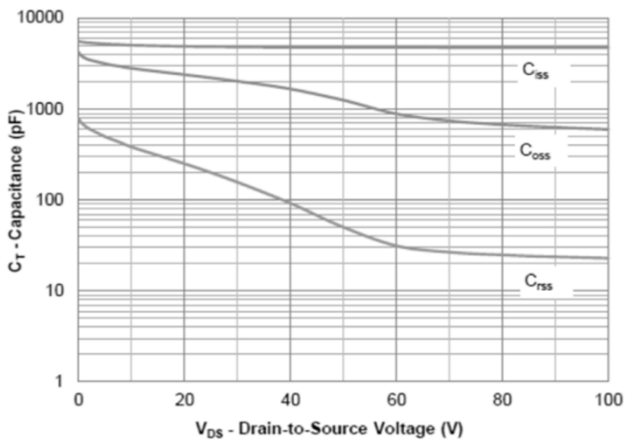


Figure 9: Capacitance Characteristics

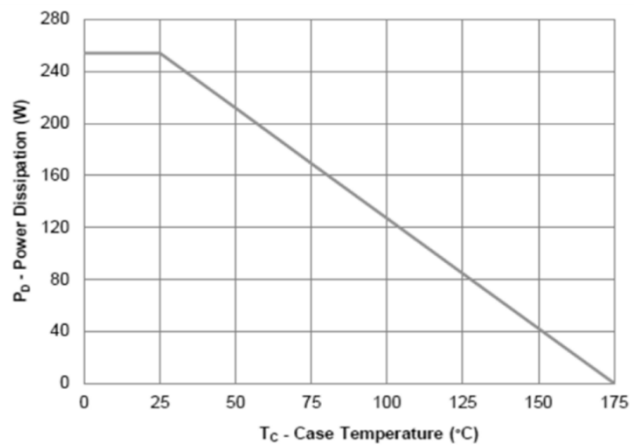


Figure 10: Power Derating

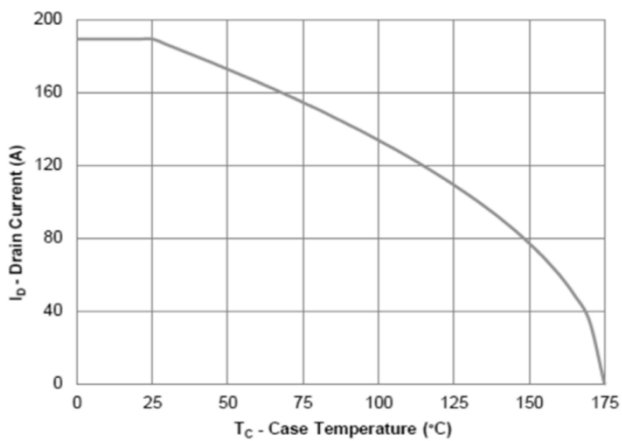


Figure 11: Current Derating

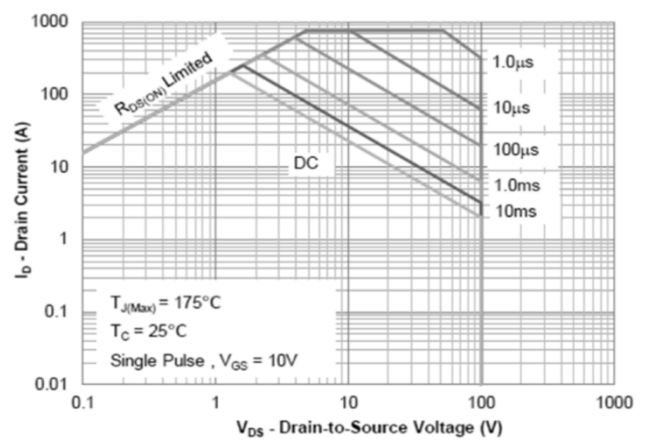


Figure 12: Safe Operating Area

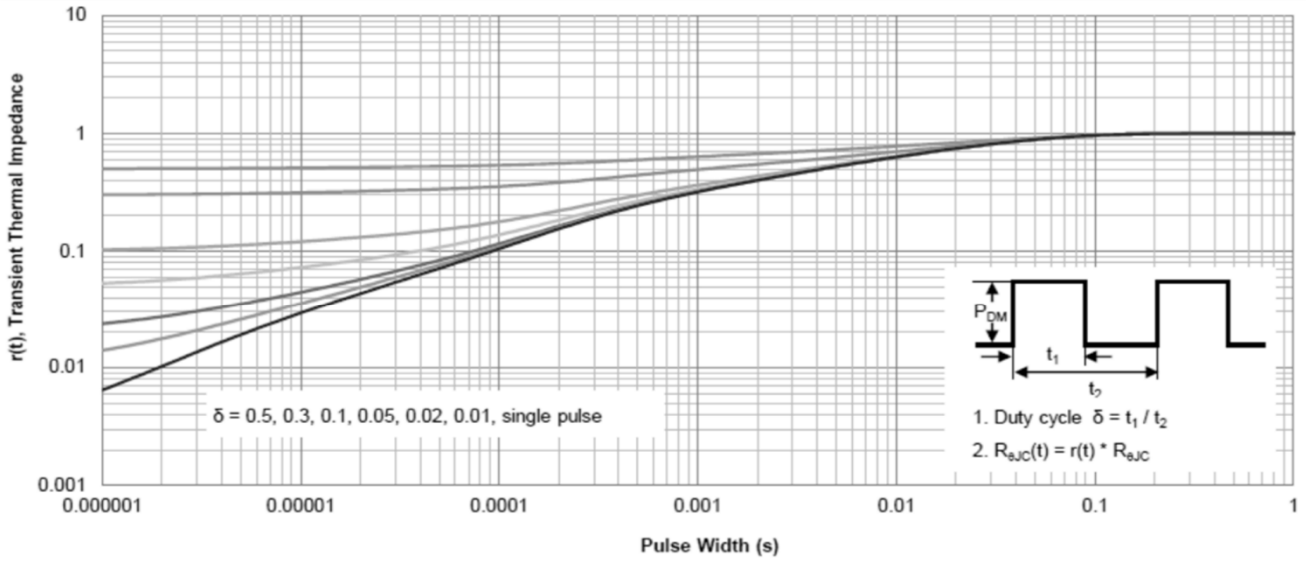
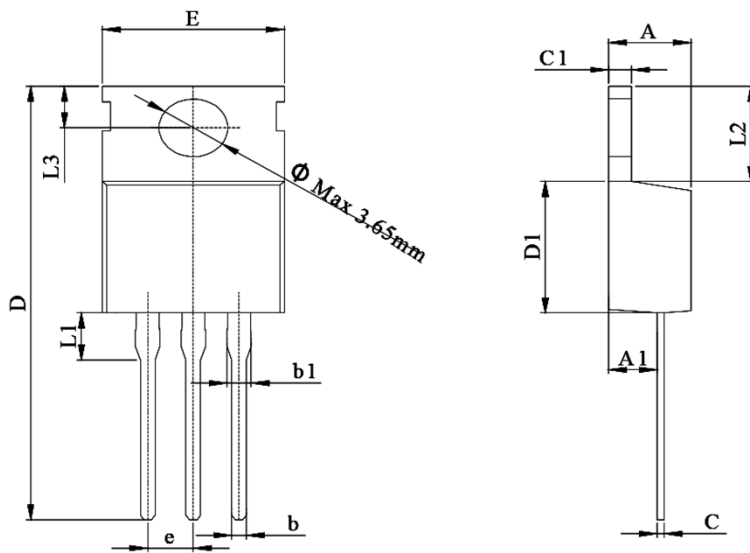



Figure 13: Normalized Maximum Transient Thermal Impedance

Product Dimension (TO-220)



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.37	4.70	0.172	0.185
A1	2.20	3.00	0.087	0.118
b	0.70	0.95	0.028	0.037
b1	1.14	1.65	0.045	0.065
C	0.45	0.60	0.018	0.024
C1	1.23	1.40	0.048	0.055
D	28.00	29.80	1.102	1.173
D1	8.90	9.90	0.350	0.390
E	9.70	10.50	0.382	0.413
L1	-	4.00	-	0.157
L2	6.25	6.90	0.246	0.272
L3	2.40	3.00	0.094	0.118
e	2.54 BSC.		0.010 Ref.	


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