

Description

The PSMTL10R1 uses split gate trench technology to provide excellent $R_{\text{DS(ON)}}$ and low gate charge. This device is suitable for power management and high efficiency applications at high switching frequencies applications.

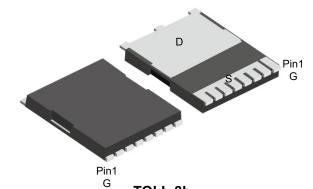
MOSFET Product Summary				
V _{DS} (V)	$R_{DS(on)}(m\Omega)$ (Typ)	$I_D(A)$		
100	1.2@ V _{GS} = 10V	415		

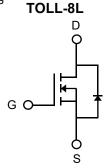
Feature

- ➤ Low R_{DS(ON)} Ensures On-State Losses are Minimized
- ➤ Excellent Q_{gd} x R_{DS(ON)} Product(FOM)
- Advanced Technology for DC-DC Converts
- Small Form Factor Thermally Efficient Package Enables Higher Density End Products
- > 100% UIS (Avalanche) Rated
- ➤ Lead-Free Finish; RoHS Compliant
- > Halogen and Antimony Free. "Green" Device

Applications

- PWM applications
- Load switch
- Power management
- > DC-DC Converters
- Wireless Chargers





Circuit Diagram



Absolute maximum rating@25°C

Rating		Symbol	Value	Units	
Drain-Source Voltage		V _{DS}	100	V	
Gate-Source Voltage		V _{GS}	±20	V	
Duain Commant Continuous 1)	T _C =25°C		415	A	
Drain Current-Continuous ¹⁾	T _C =100°C	- I _D	293		
Pulsed Drain Current ²⁾		I _{DM}	1589	А	
T. (15 5: 1: 4)	T _C =25°C		500	W	
Total Power Dissipation ⁴⁾	T _C =100°C	$ P_D$	250		
Avalanche Current @ L=0.3mH	•	I _{AS}	78	Α	
Avalanche Energy @ L=0.3mH		E _{AS}	913	mJ	
Thermal Resistance , Junction-to-Ca	ase ⁴⁾	$R_{ heta JC}$	0.3	°C/W	
Thermal Resistance Junction-to-Am	bient ³⁾	$R_{\theta JA}$	25	°C/W	
Junction and Storage Temperature F	Range	$T_{J_i}T_{STG}$	-55~+150	°C	

Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units	
Off Characteristics							
Drain-Source Breakdown Voltage	BV _{DSS}	$V_{GS} = 0V, I_{D} = 250\mu A$	100	-	-	V	
Zana Cata Valta na Busin Comunit	re Voltage Drain Current $V_{DS} = 100V$, $T_J = 25^{\circ}C$		-	-	1.0		
Zero Gate Voltage Drain Current	l _{DSS}	$V_{GS} = 0V$ $T_J = 55^{\circ}C$	-	-	10	μA	
Gate-Body Leakage Current	I _{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	±100	nA	
On Characteristics ⁵⁾	On Characteristics ⁵⁾						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0	3.0	4.0	V	
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V,I _D = 20A	-	1.2	1.5	mΩ	
Forward Transconductance	g _{fs}	$V_{DS} = 5 \text{ V,I}_{D} = 20 \text{A}$	-	72	-	S	
Diode Forward Voltage	V _{SD}	V _{GS} = 0V,I _S = 1A	-	0.7	1.2	V	
Dynamic Characteristics ⁶⁾							
Input Capacitance	C _{lss}		-	11930	-	pF	
Output Capacitance	C _{oss}	$V_{DS} = 50V, V_{GS} = 0V,$ f = 1.0MHz	-	2720	-		
Reverse Transfer Capacitance	C _{rss}		-	71	-		
Switching Characteristics ⁶⁾							
Turn-on Delay Time	t _{d(on)}		-	26	-	- ns	
Turn-on Rise Time	t _r	$V_{DS} = 50V, V_{GS} = 10V,$	-	35	-		
Turn-Off Delay Time	t _{d(off)}	$R_{G} = 3\Omega, I_{D} = 20A$	-	94	-		
Turn-Off Fall Time	t _f		-	49	-		
Total Gate Charge @ V _{GS} = 10V	0		-	154	-		
Total Gate Charge @ V _{GS} = 6V	Q_{g}	$V_{DS} = 50V, I_{D} = 20A,$	-	98	-		
Gate-Source Charge	Q_{gs}	$V_{GS} = 10V$,	-	46	-	nC	
Gate-Drain Charge	Q_{gd}		-	29	-		
Gate Resistance	R_g	V _{GS} =0V,V _{DS} =0V,f=1MHz	_	1.6	-	Ω	
Drain-Source Diode Characteristics ⁶⁾							
Reverse Recovery Time	t _{rr}	1 = 20.0 d/d = 400.0/	_	107	-	ns	
Reverse Recovery Charge	Q_{rr}	- I _F =20A, d _i /d _t =100A/μs		229	-	nC	
Diode Forward Current	I _s	-	-	-	415	Α	

Notes

- 1. Pulse width limited by maximum junction temperature.
- Pulse test: Pulse width ≤ 100µs, duty cycle ≤ 2%.
- 3. Device mounted on 1 inch FR4 PCB with 2oz.Copper.
- 4. Device mounted on infinite heatsink.
- Measured under pulsed conditions. Pulse width ≤ 300µs, duty cycle ≤ 2%.
- 6. Guaranteed by design, not subject to production.

Typical Characteristics

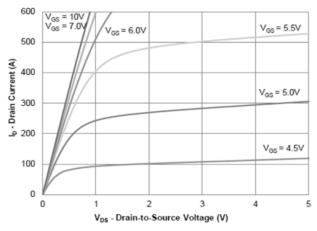


Figure 1: Output Characteristics

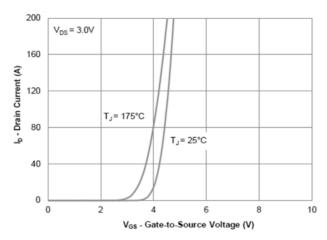


Figure 2: Transfer Characteristics

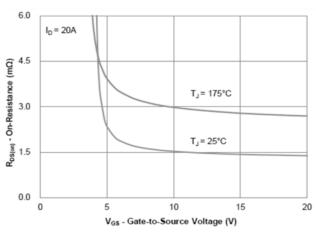


Figure 3: On-Resistance vs. Gate-Source Voltage

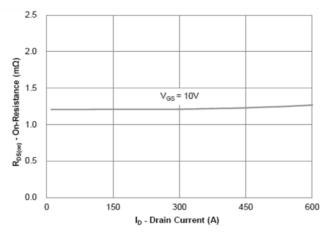


Figure 4: On-Resistance vs. Gate-Source Voltage

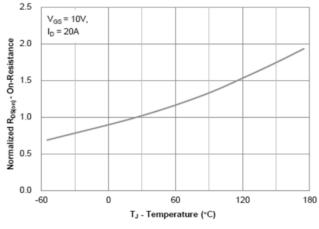


Figure 5: On-Resistance vs. Junction Temperature

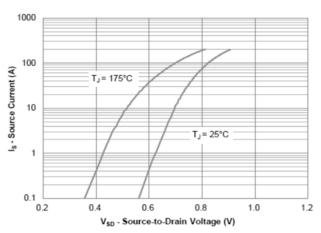


Figure 6: Source-Drain Diode Forward Voltage

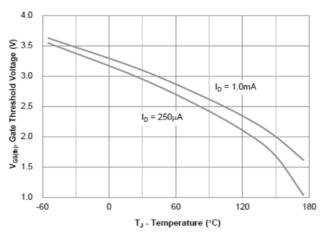


Figure 7: Gate Threshold Variation vs. Junction Temperature

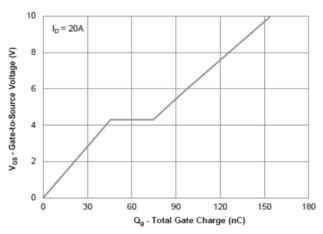


Figure 8: Gate Charge Characteristics

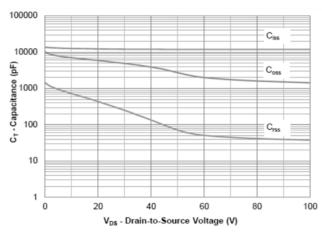


Figure 9: Capacitance Characteristics

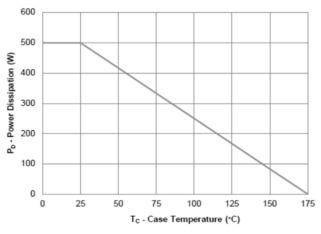


Figure 10: Power Derating

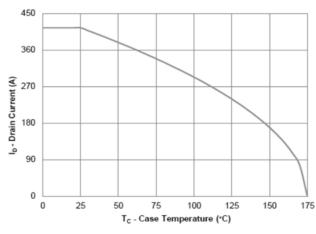


Figure 11: Current Derating

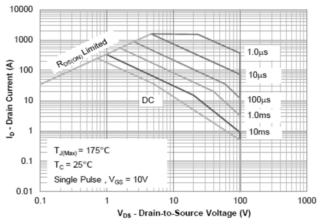


Figure 12: Safe Operating Area

PSMTL10R1

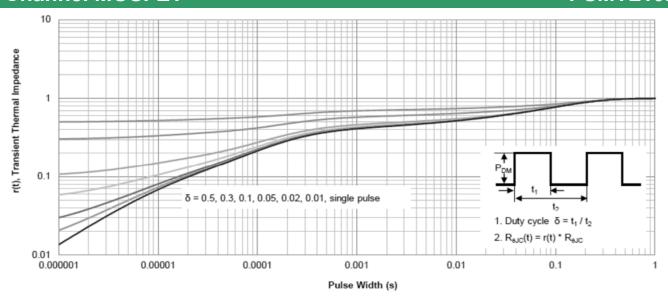
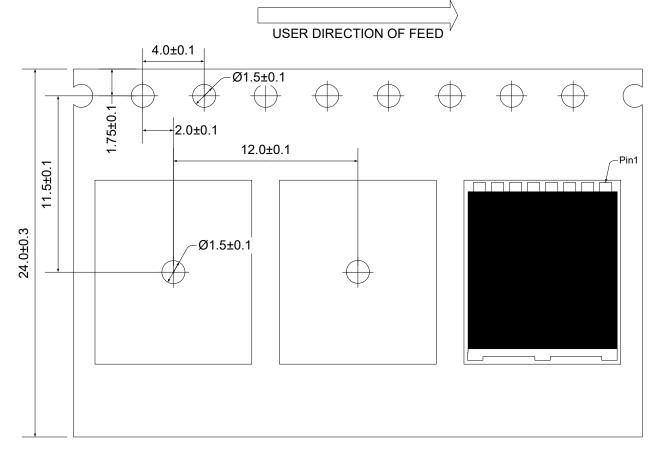


Figure 13: Normalized Maximum Transient Thermal Impedance

Ordering Information

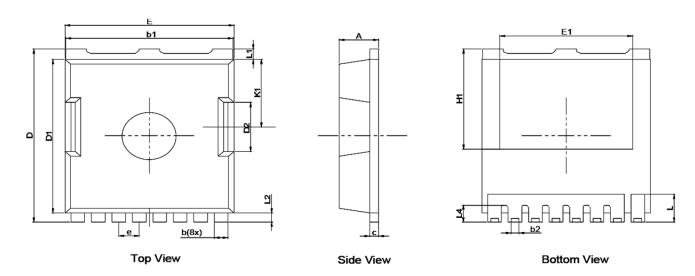
Device	Package	Reel	Shipping
PSMTL10R1	TOLL-8L	13"	2000 / Tape & Reel

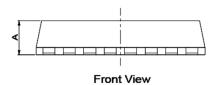
Load With Information

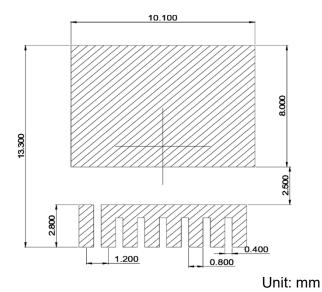


Unit:mm

Product Dimension (TOLL-8L)







Suggested PCB Layout

Di	Millim	neters	Inches		
Dim	Min	Max	Min	Max	
А	2.20	2.40	0.087	0.094	
b	0.65	0.90	0.026	0.035	
b1	9.65	9.95	0.380	0.392	
С	0.40	0.60	0.016	0.024	
D	11.48	11.95	0.452	0.470	
D1	10.25	10.70	0.404	0.421	
D2	2.85	3.40	0.112	0.134	
E	9.70	10.10	0.382	0.398	
E1	8.00	9.25	0.315	0.364	
е	1.20 BSC		0.047 BSC		
H1	6.70	7.30	0.264	0.287	
K1	4.55 BSC		0.179 BSC		
L	1.35	2.10	0.053	0.083	
L1	0.70 BSC		0.028 BSC		
L2	0.60 BSC		0.024 BSC		
L4	0.95	1.35	0.037	0.053	

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