Prisemi®

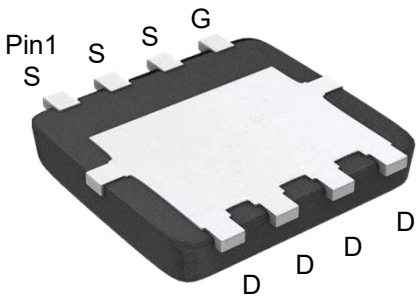
PSM8N04R1H

N-Channel MOSFET

Description

The PSM8N04R1H uses split gate trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for power management and high efficiency applications at high switching frequencies applications.

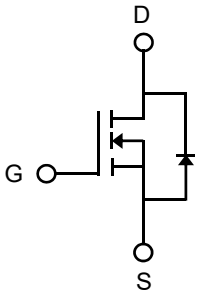
MOSFET Product Summary		
V_{DS}(V)	$R_{DS(on)}$(mΩ)(Typ)	I_D(A)
40	1.2@ V_{GS} = 10V	212



PDFN5060-8L
(Bottom View)

Feature

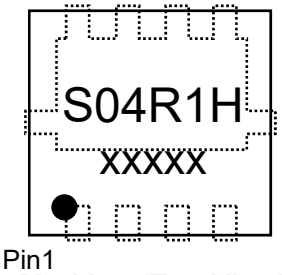
- Low $R_{DS(ON)}$ - Ensures On-State Losses are Minimized
- Excellent Q_{gd} x $R_{DS(ON)}$ Product(FOM)
- Advanced Technology for DC-DC Converts
- Small Form Factor Thermally Efficient Package Enables Higher Density End Products
- 100% UIS (Avalanche) Rated
- Lead-Free Finish ; RoHS Compliant
- Halogen and Antimony Free. "Green" Device



Circuit Diagram

Applications

- PWM applications
- Load switch
- Power management
- DC-DC Converters
- Wireless Chargers



Marking (Top View)

Absolute maximum rating@25℃

Rating		Symbol	Value	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous[1]	T_C=25℃	I_D	212	A
	T_C=100℃		134	
Pulsed Drain Current[2]		I_{DM}	850	A
Total Power Dissipation	T_C=25℃	P_D	104	W
	T_C=100℃		42	
Avalanche Current @ L=0.1mH		I_{AS}	56	A
Avalanche Energy @ L=0.1mH[3]		E_{AS}	436	mJ
Thermal Resistance , Junction-to-Case[5]		$R_{\theta JC}$	1.2	℃/W
Thermal Resistance Junction-to-Ambient[4]		$R_{\theta JA}$	45	℃/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55~+150	℃

Electrical characteristics per line@25℃ (unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Off Characteristics[6)]							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V,I_D = 250μA		40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V	T_J=25℃	-	-	1.0	μA
			T_J=125℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS} = ±20V,V_{DS} = 0V		-	-	±100	nA
On Characteristics[6)]							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS},I_D = 250μA		2.0	3.0	4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 10V,I_D = 20A		-	1.2	1.4	mΩ
Forward Transconductance	g_{fs}	V_{DS} = 5 V,I_D = 20A		-	34	-	S
Diode Forward Voltage	V_{SD}	V_{GS} = 0V,I_S = 2A		-	0.7	1.2	V
Dynamic Characteristics[7)]							
Input Capacitance	C_{lss}	V_{DS} = 20V,V_{GS} = 0V, f = 1.0MHz		-	3073	-	pF
Output Capacitance	C_{oss}			-	1515	-	
Reverse Transfer Capacitance	C_{rss}			-	58	-	
Gate Resistance	R_g	V_{GS}=0V,V_{DS}=0V,f=1MHz		-	1.4	-	Ω
Switching Characteristics[7)]							
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 20V, V_{GS} = 10V, R_G = 3Ω, I_D = 20A		-	5.6	-	ns
Turn-on Rise Time	t_r			-	15	-	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Turn-Off Fall Time	t_f			-	9.9	-	
Total Gate Charge @ V_{GS} = 10V	Q_g	V_{DS} = 20V, I_D = 20A, V_{GS} = 10V		-	41	-	nC
Total Gate Charge @ V_{GS} = 6V				-	26	-	
Gate-Source Charge	Q_{gs}			-	14	-	
Gate-Drain Charge	Q_{gd}			-	7.5	-	
Gate Plateau Voltage	$V_{plateau}$			-	5.0	-	V
Drain-Source Diode Characteristics[6)]							
Reverse Recovery Time	t_{rr}	I_F=20A, d_i/d_t=100A/μs		-	46	-	ns
Reverse Recovery Charge	Q_{rr}			-	50	-	nC
Diode Forward Current	I_S	-		-	-	132	A

Notes:
1. This current is chip limited, which is calculated based on $R_{\theta JC}$
2. This current is calculated on single pulse with 10μs Pulse & Duty Cycle = 1%.
3. Defined by design, not subject to production test, E_{AS} condition: T_J=25°C, V_{DD}=20V, V_{GS}=10V, L=1.0mH.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Characteristics

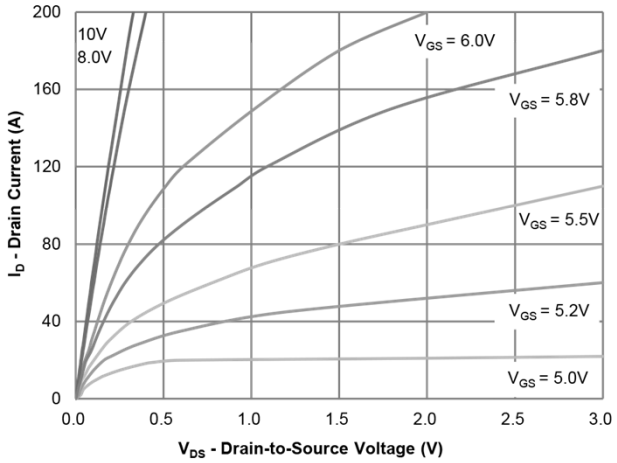


Figure 1: Output Characteristics

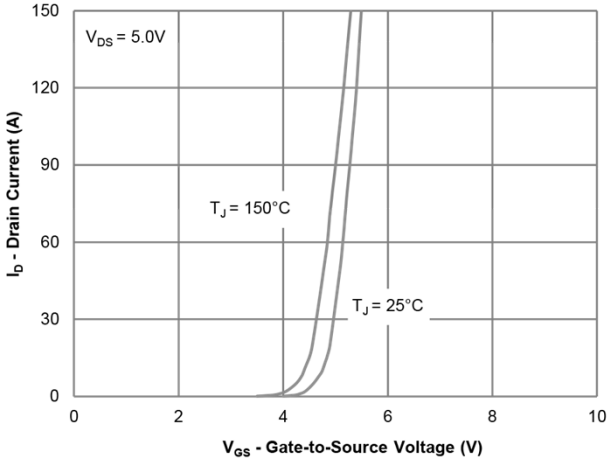


Figure 2: Transfer Characteristics

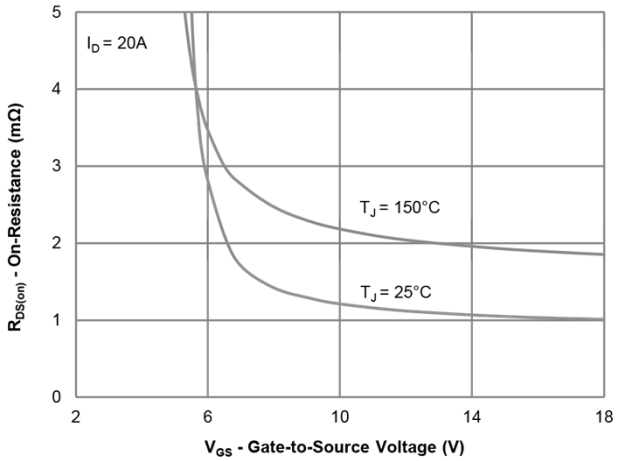


Figure 3: On-Resistance vs. Gate-Source Voltage

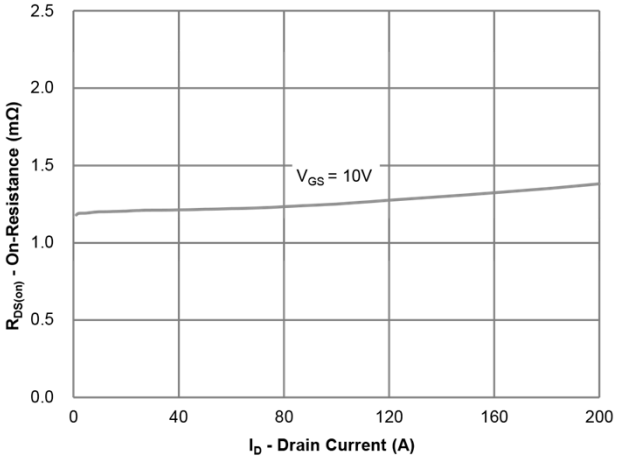


Figure 4: On-Resistance vs. Gate-Source Voltage

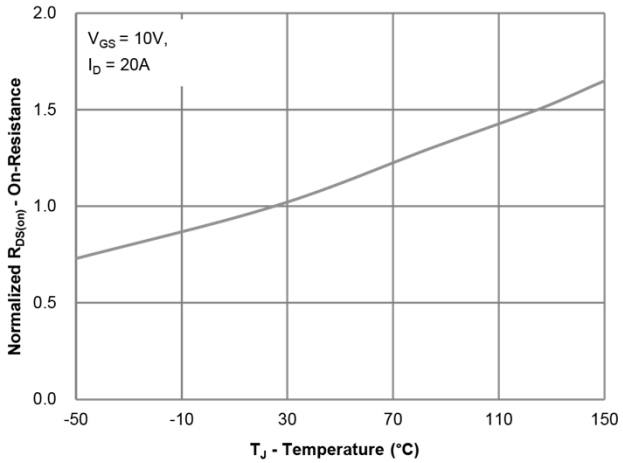


Figure 5: On-Resistance vs. Junction Temperature

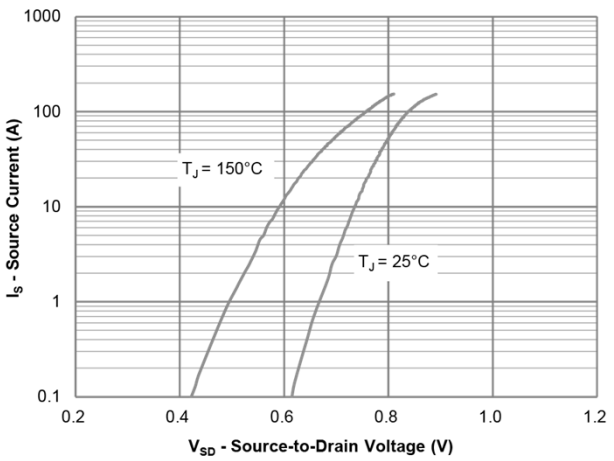


Figure 6: Source-Drain Diode Forward Voltage

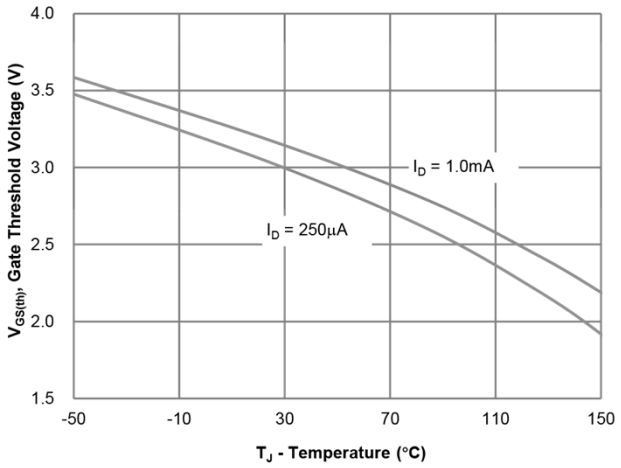


Figure 7: Gate Threshold Variation vs. Junction Temperature

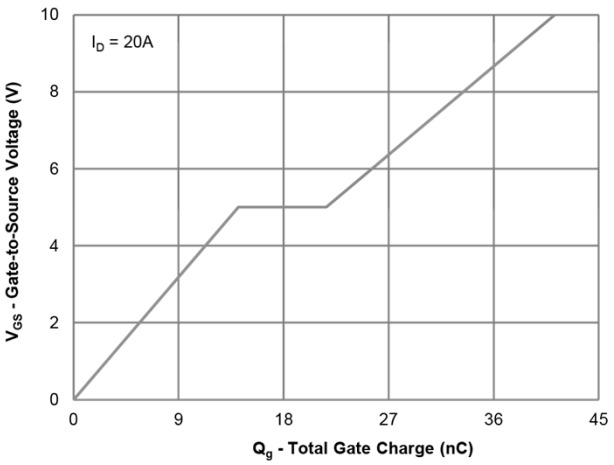


Figure 8: Gate Charge Characteristics

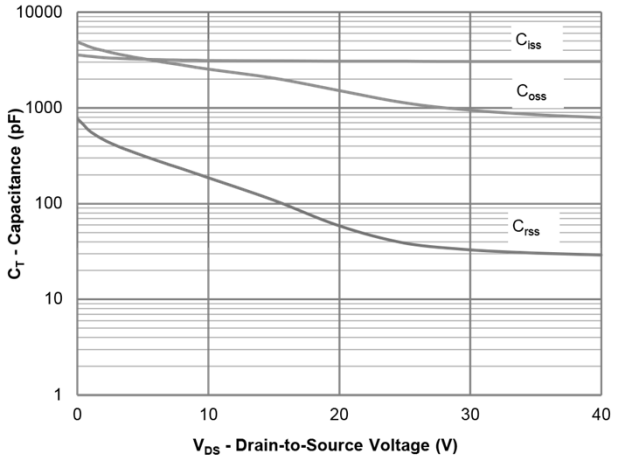


Figure 9: Capacitance Characteristics

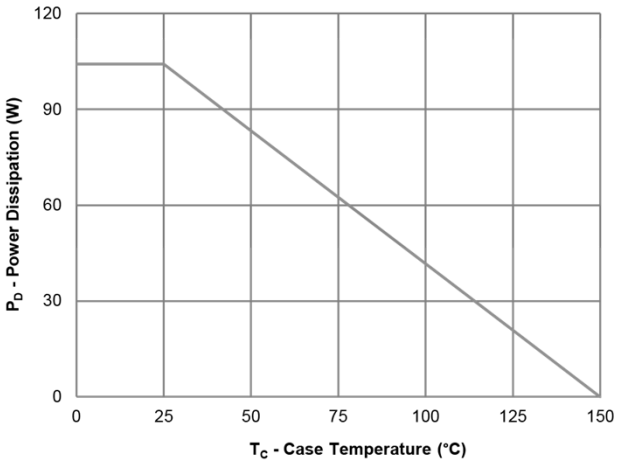


Figure 10: Power Derating

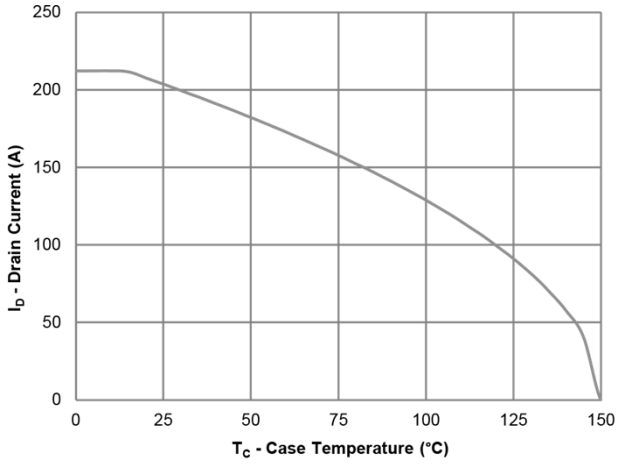


Figure 11: Current Derating

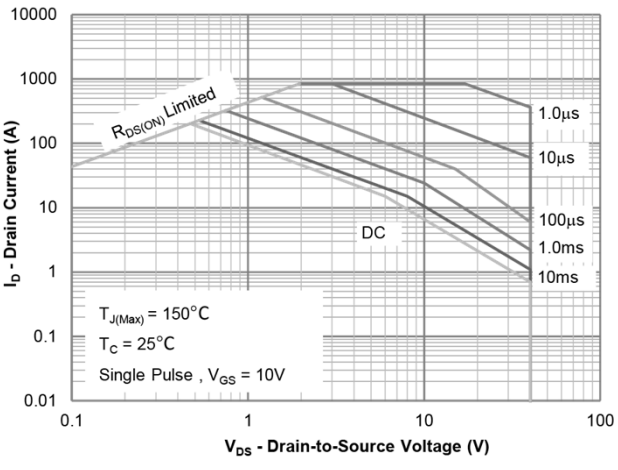


Figure 12: Safe Operating Area

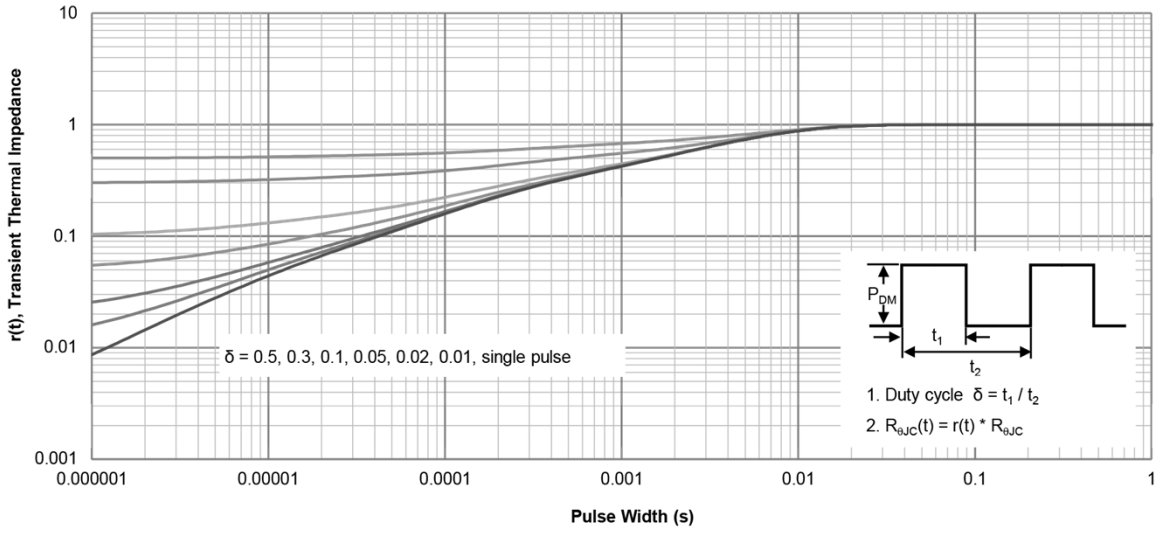
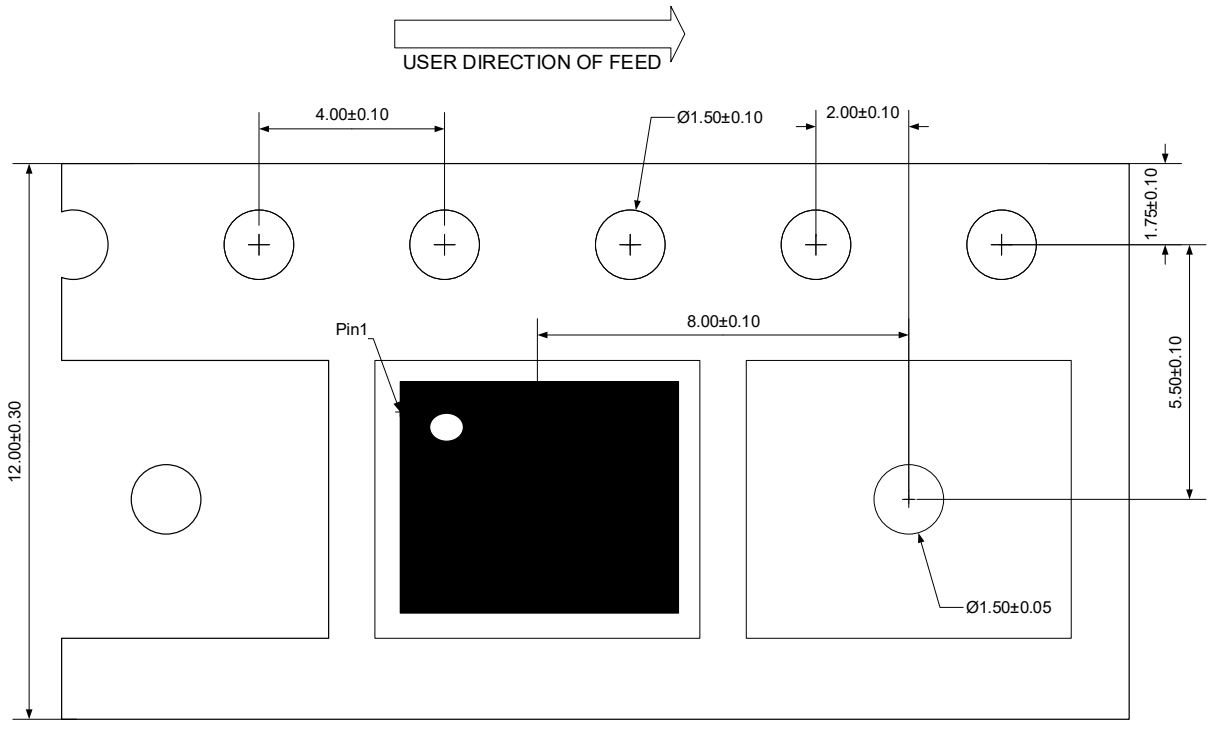


Figure 13: Normalized Maximum Transient Thermal Impedance

Ordering Information

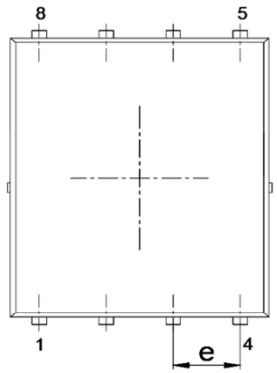
Device	Package	Reel	Shipping
PSM8N04R1H	PDFN5060-8L	13"	5000 / Tape & Reel

Load With Information

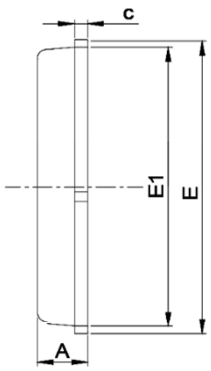


Unit:mm

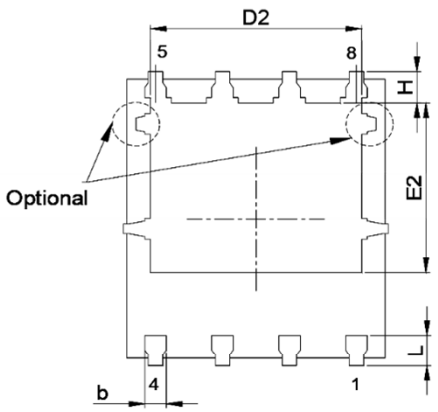
Product Dimension (PDFN5060-8L)



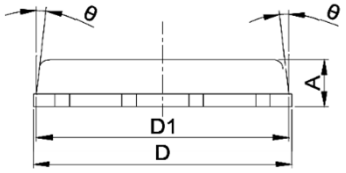
Top View



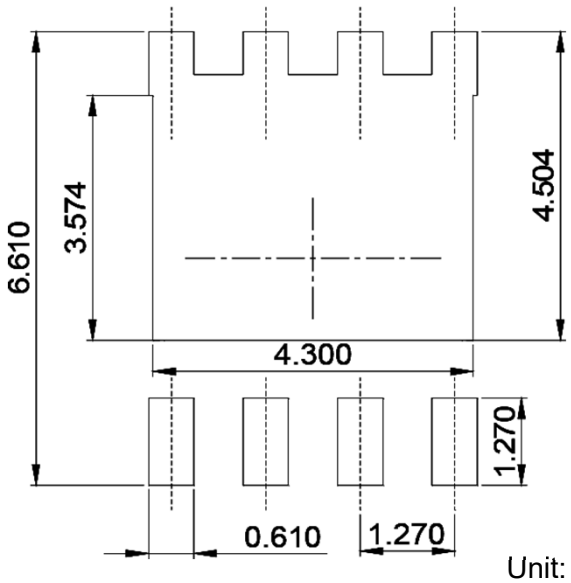
Side View



Bottom View



Front View



Unit: mm

Suggested PCB Layout

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.10	0.035	0.043
b	0.20	0.51	0.008	0.020
c	0.21	0.34	0.008	0.013
D	4.90	5.40	0.193	0.213
D1	4.80	5.15	0.189	0.203
D2	3.91	4.20	0.154	0.165
E	5.90	6.50	0.232	0.256
E1	5.65	5.95	0.222	0.234
E2	3.32	3.63	0.131	0.143
e	1.27 BSC.		0.050 Ref.	
H	0.50	0.93	0.020	0.037
L	0.45	0.91	0.018	0.036
θ	0°	12°	0°	12°

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