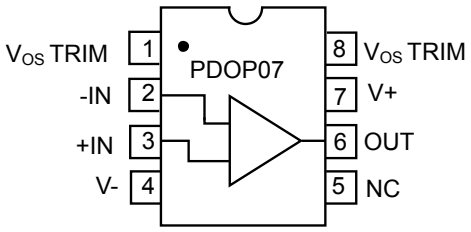
Ultralow Offset Voltage Operational Amplifiers

Feature

- Low V_O:75μV Max
- Low V_{OS} Drift:1.3μV/℃ Max
- Ultra-Stable vs. Time:1.5μV/Month Max
- Low Noise: 0.6μV p-p Max
- Wide Input Voltage Range:±14V
- Wide Supply Voltage Range:3V to 18V
- 125℃ Temperature-Tested Dice

Pin Connections

SOIC-8



NC=No Connect

Application

- Wireless Base Station Control Circuits
- Optical Network Control Circuits
- Instrumentation
- Sensors and Controls

  Thermocouples

  RTDs

  Strain Bridges

  Shunt Current Measurements
- Precision Filters

General Description

The PDOP07 has very low input offset voltage (75 μV max for PDOP07E) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The PDOP07 also features low input bias current (±1.2nA for PDOP07E) and high open-loop gain (200 V/mV for PDOP07E). The low offsets and high open-loop gain make the PDOP07 particularly useful for high-gain instrumentation applications. The wide input voltage range of ±13 V minimum combined with high CMRR of 106 dB (PDOP07E) and high input impedance provides high accuracy in the no inverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains. Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the PDOP07, even at high gain, combined with the freedom from external nulling have made the PDOP07 an industry standard for instrumentation applications. The PDOP07 is available in two standard performance grades. The PDOP07E is specified for operation over the 0°C to 70°C range, and PDOP07C over the –40°C to +85°C temperature range.

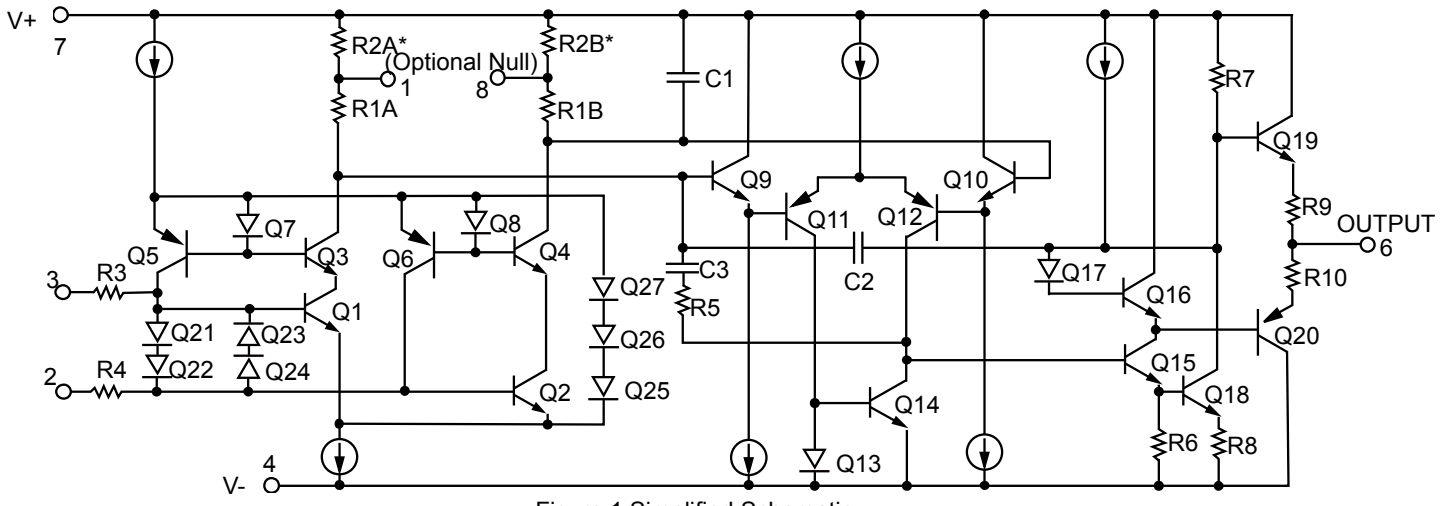


Figure 1.Simplified Schematic

PDOP07E Electrical Characteristics

(V_S=±15V,T_A=25℃， unless otherwise noted.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Characteristics						
Input Offset Voltage[1]	V_{OS}			30	75	μV
Long-Term V_{OS} Stability[2]	V_{OS}/Time			0.3	1.5	μV/Mo
Input Offset Current	I_{OS}			0.5	3.8	nA
Input Bias Current	I_B			±1.2	±4.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.35	0.6	μV p-p
Input Noise Voltage Density	e_n	f_o=10Hz f_o =100Hz[3] f_o =1kHz		10.3 10.0 9.6	18.0 13.0 11.0	nV√Hz nV√Hz nV√Hz
Input Noise Current	I_n p-p			14	30	pA p-p
Input Noise Current Density	I_n	f_o =10Hz f_o =100Hz[3] f_o =1kHz		0.32 0.14 0.12	0.80 0.23 0.17	pA√Hz pA√Hz pA√Hz
Input Resistance-Differential Mode[4]	R_{IN}		15	50		mΩ
Input Resistance-Common-Mode	R_{INCM}			160		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13V	106	123		dB
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18V		5	20	μV/V
Large-Signal Voltage Gain	A_{VO}	R_L≥2KΩ,V_O=±10V R_L≥500Ω,V_O=±0.5V, V_S=±3V[4]	200 150	500 400		V/mV V/mV
Output Characteristics						
Output Voltage Swing	V_O	R_L≥10KΩ R_L≥2KΩ R_L≥1 KΩ	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V V V
Dynamic Performance						
Slew Rate	SR	R_L≥2 KΩ[3]	0.1	0.3		V/μS
Closed-Loop Bandwidth	BW	A_{VOL}=1[5]	0.4	0.6		MHz
Closed-Loop Output Resistance	R_O	V_O=0,I_O=0		60		Ω
Power Consumption	P_d	V_S=±15V,No Load V_S=±13V,No Load		75 4	120 6	mW mW
Offset Adjustment Range		R_P=20 KΩ		±4		mV

NOTES

1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

2: Long-term input offset voltage stability refers to the averaged trend time of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial

hour of operation, changes in VOS during the first 30 operating days are typically 2.5 μV refer to the typical performance curves. Parameter is sample tested.

3: Sample tested.

4: Guaranteed by design.

5: Guaranteed but not tested.

Specifications subject to change without notice

PDOP07E Electrical Characteristics

(V_S=±15V,0℃≤T_A≤70℃， unless otherwise noted.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Characteristics						
Input Offset Voltage[1]	V_{OS}			45	130	μV
Voltage Drift without External Trim[2]	TCV_{OS}			0.3	1.3	μV/℃
Voltage Drift with External Trim[3]	TCV_{OSN}	R_P=20 KΩ		0.3	1.3	μV/℃
Input Offset Current	I_{OS}			0.9	5.3	nA
Input Offset Current Drift	TCI_{OS}			8	35	pA/℃
Input Bias Current	I_B			±1.5	±5.5	nA
Input Bias Current Drift	TCI_B			13	35	pA/℃
Input Voltage Range	I_{VR}		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13V	103	123		dB
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18V		7	32	μV/V
Large-signal Voltage Gain	A_{VO}	R_L≥2KΩ,V_O= ±10V	180	450		V/mV
Output Characteristics						
Output Voltage Swing	V_O	R_L≥10KΩ	±12	±12.6		V

NOTES

1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

2: Guaranteed by design.

3: Sample tested.

Specifications subject to change without notice.

PDOP07C Electrical Characteristics

(V_S=±15V,T_A=25℃， unless otherwise noted.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Characteristics						
Input Offset Voltage[1]	V_{OS}			60	150	μV
Long-Term V_{OS} Stability[2]	V_{OS}/Time			0.4	2.0	μV/Mo
Input Offset Current	I_{OS}			0.8	6.0	nA
Input Bias Current	I_B			±1.8	±7.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.38	0.65	μV p-p
Input Noise Voltage Density	e_n	f_o=10Hz f_o =100Hz[3] f_o =1kHz		10.5 10.2 9.8	20.0 13.5 11.5	nV√Hz nV√Hz nV√Hz
Input Noise Current	I_n p-p			15	35	pA p-p
Input Noise Current Density	I_n	f_o =10Hz f_o =100Hz[3] f_o =1kHz		0.35 0.15 0.13	0.90 0.27 0.18	pA√Hz pA√Hz pA√Hz
Input Resistance-Differential Mode[4]	R_{IN}		8	33		mΩ
Input Resistance-Common-Mode	R_{INCM}			120		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13V	100	120		dB
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18V		7	32	μV/V
Large-Signal Voltage Gain	A_{VO}	R_L≥2KΩ,V_O=±10V R_L≥500Ω,V_O=±0.5V, V_S=±3V[4]	120 100	400 400		V/mV V/mV
Output Characteristics						
Output Voltage Swing	V_O	R_L≥10KΩ R_L≥2KΩ R_L≥1 KΩ	±12.0 ±11.5	±13.0 ±12.8 ±12.0		V V V
Dynamic Performance						
Slew Rate	SR	R_L≥2 KΩ[3]	0.1	0.3		V/μS
Closed-Loop Bandwidth	BW	A_{VOL}=1[5]	0.4	0.6		MHz
Closed-Loop Output Resistance	R_O	V_O=0,I_O=0		60		Ω
Power Consumption	P_d	V_S=±15V,No Load V_S=±13V,No Load		80 4	150 8	mW mW
Offset Adjustment Range		R_P=20 KΩ		±4		mV

NOTES

1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

2: Long-term input offset voltage stability refers to the averaged trend time of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial

hour of operation, changes in VOS during the first 30 operating days are typically 2.5 μV refer to the typical performance curves. Parameter is sample tested.

3:Sample tested.

4: Guaranteed by design.

5: Guaranteed but not tested.

Specifications subject to change without notice.

PDOP07C Electrical Characteristics

(V_S=±15V,-40℃≤T_A≤+85℃，unless otherwise noted.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Characteristics						
Input Offset Voltage[1]	V_{OS}			85	250	μV
Voltage Drift without External Trim[2]	TCV_{OS}			0.5	1.8	μV/℃
Voltage Drift with External Trim[3]	TCV_{OSN}	R_P=20 KΩ		0.4	1.8	μV/℃
Input Offset Current	I_{OS}			1.6	8.0	nA
Input Offset Current Drift	TCI_{OS}			12	50	pA/℃
Input Bias Current	I_B			±2.0	±9.0	nA
Input Bias Current Drift	TCI_B			18	50	pA/℃
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13V	97	120		dB
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18V		10	51	μV/V
Large-signal Voltage Gain	A_{VO}	R_L≥2KΩ,V_O= ±10V	100	400		V/mV
Output Characteristics						
Output Voltage Swing	V_O	R_L≥10KΩ	±11	±12.6		V

NOTES

1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

2: Guaranteed by design.

3: Sample tested.

Specifications subject to change without notice.

Absolute Maximum Ratings*

Supply Voltage(V_S)…….. ±22V
Input Voltage*…….±22V
Differential Input Voltage…….±30V
Output Short-Circuit Duration……..Indefinite
Storage Temperature Range
S,P Packages……..-65℃ to +125℃
Operating Temperature Range
PDOP07E……..0℃ to 70℃
PDOP07C……....-40℃ to +85℃
Junction Temperature Range……..…150℃
Lead Temperature Range(Soldering,60sec)…300℃
*For supply voltages less than ± 22 V, the absolute maximum input voltage is equal to the supply voltage.

Package Type	θ_{JA}*	θ_{JC}	Units
8-Lead Plastic DIP(P)	103	43	℃/W
8-Lead SOIC(S)	158	43	℃/W

*θ_{JA} is specified for worst case conditions,i.e., θ_{JA} is specified for device in socket for P-DIP package, θ_{JA} is specified for device soldered to printed circuit board for SO package.

Ordering guide

Model	Temperature Range	Package Description	Package Option	Branding Information
PDOP07EP	0℃ to 70℃	8-Lead Epoxy DIP	P-8	
PDOP07CP	-40℃ to 85℃	8-Lead Epoxy DIP	P-8	
PDOP07CS	-40℃ to 85℃	8-Lead SOIC	S-8	

Caution

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the PDOP07 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Performance Characteristics

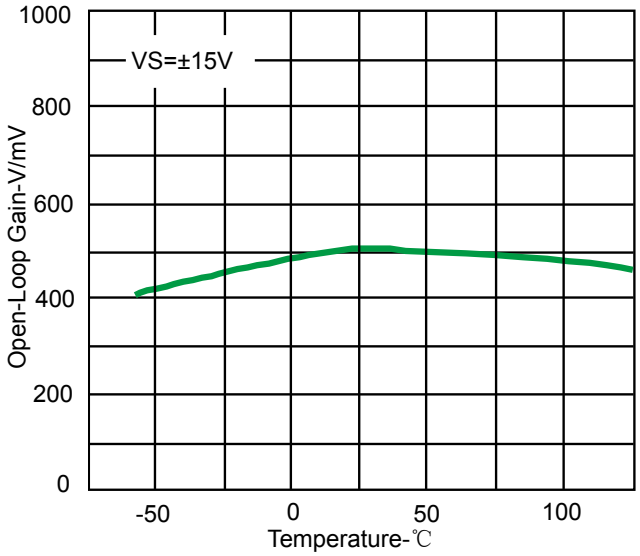


Figure 2. Open-Loop Gain vs. Temperature

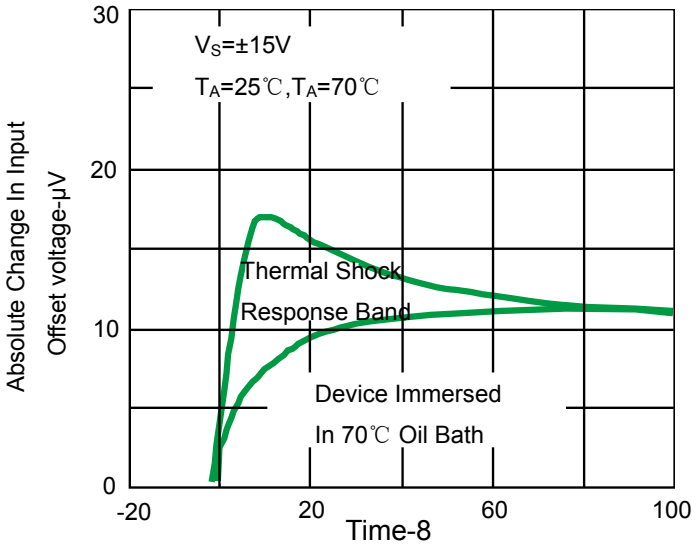


Figure 3. Offset Voltage Change Due to Thermal Shock

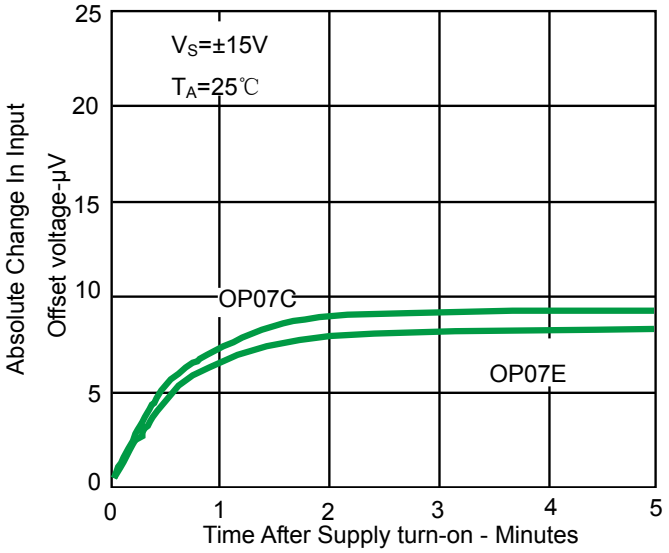


Figure4. Warm-Up Drift

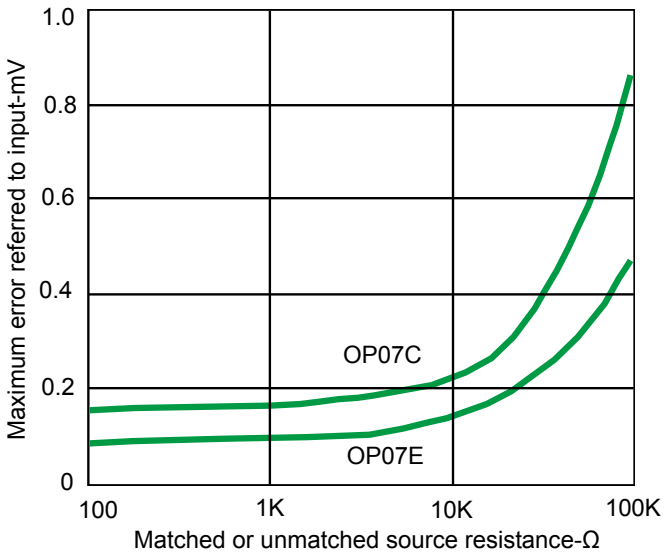


Figure 5. Maximum Error vs. Source Resistance

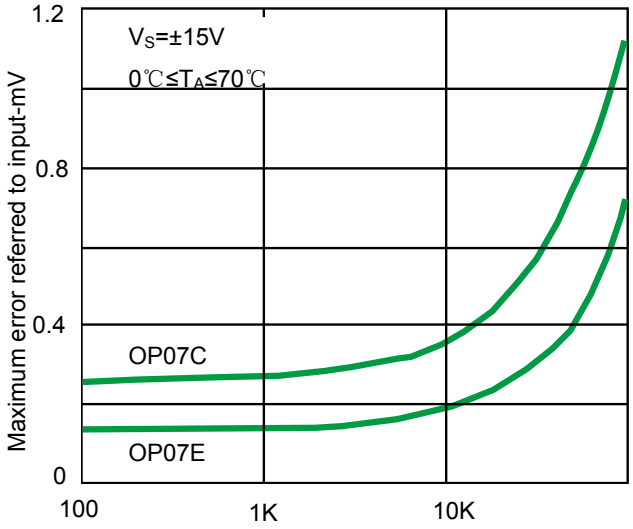


Figure 6.Maximum Error vs. Source Resistance

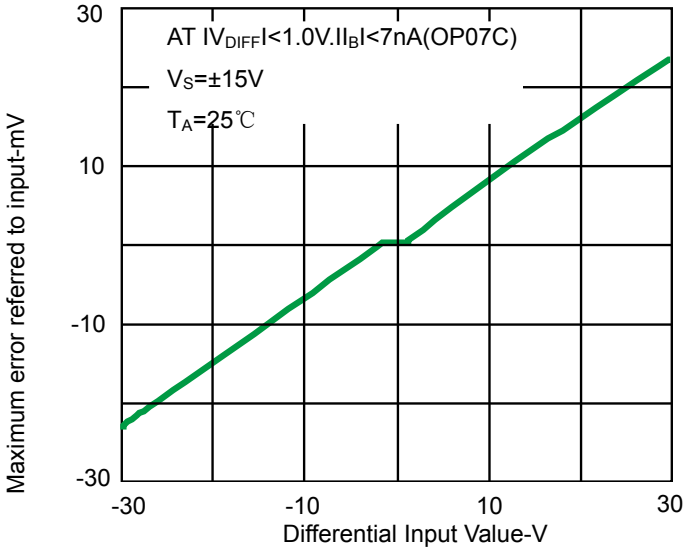


Figure 7.Input Bias Current vs. Differential Input Voltage

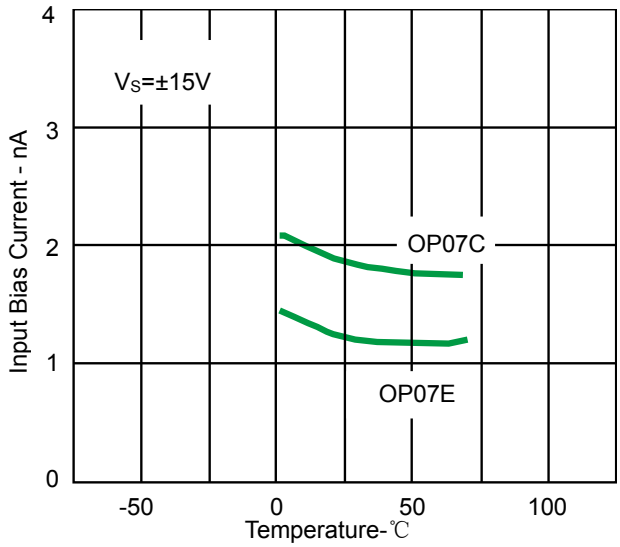


Figure 8.Input Bias Current vs. Temperature

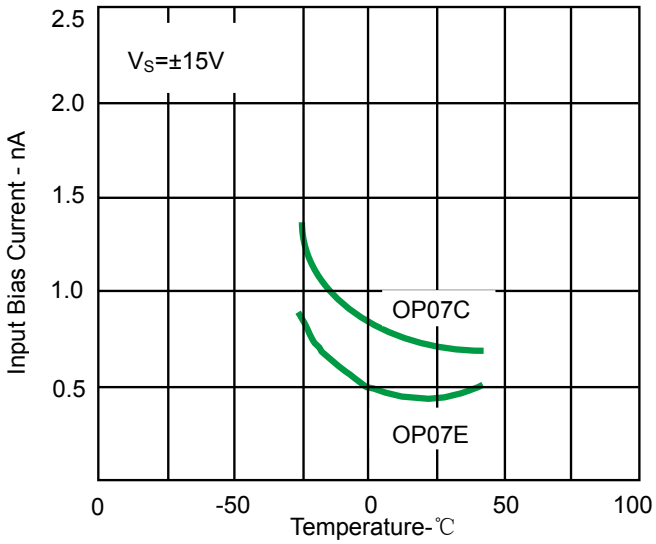


Figure 9.Input Offset Current vs. Temperature

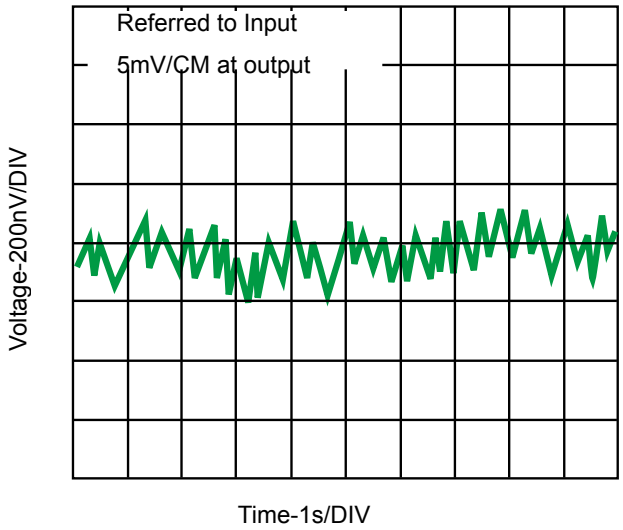


Figure 10.Low Frequency Noise

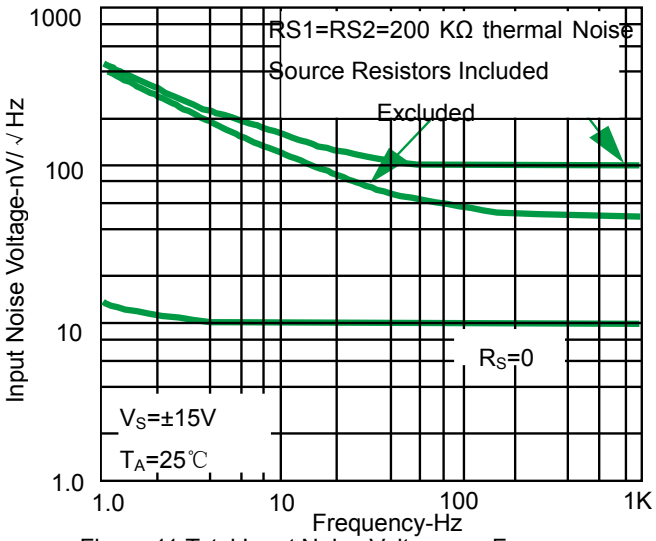


Figure 11.Total Input Noise Voltage vs. Frequency

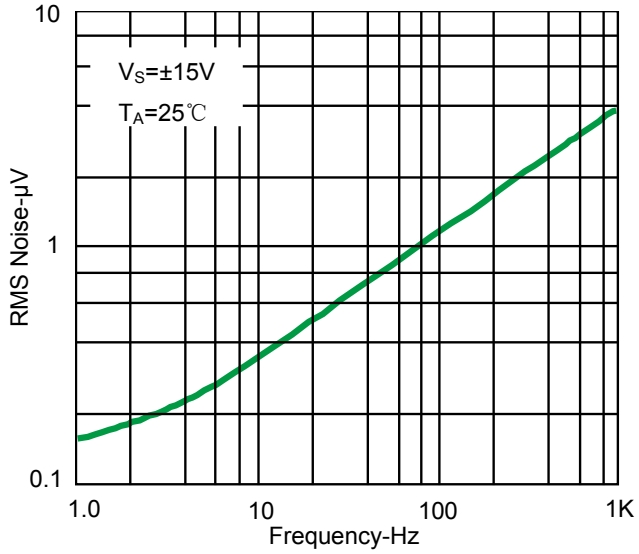


Figure 12.Input Wideband Noise vs. Bandwidth(0.1Hz to

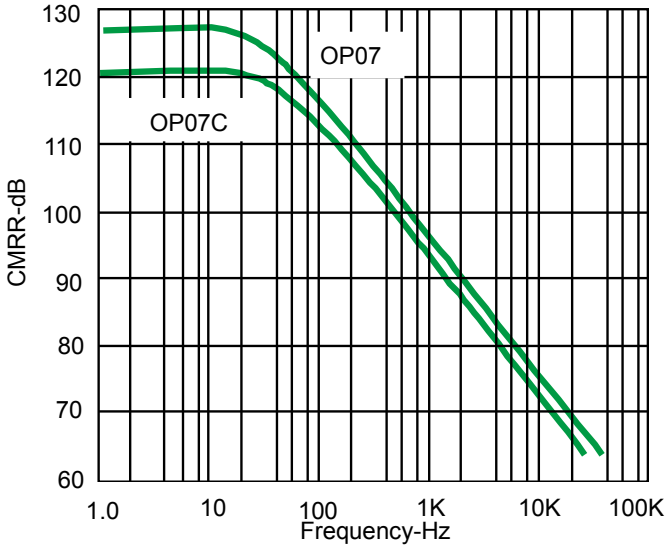


Figure 13.CMRR vs. Frequency Frequency Indicated)

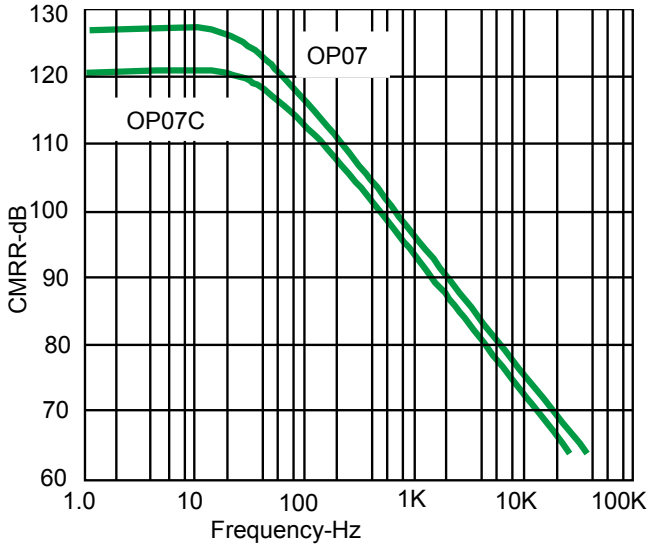


Figure 14.PSRR vs. Frequency

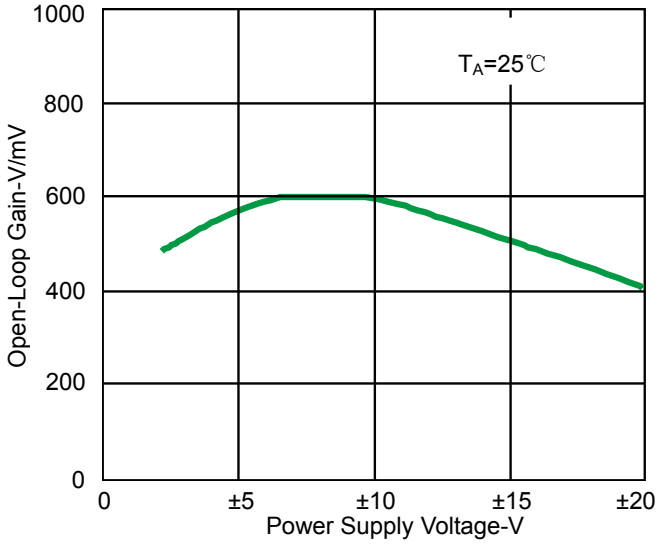


Figure 15. Open-Loop Gain vs. Power Supply Voltage

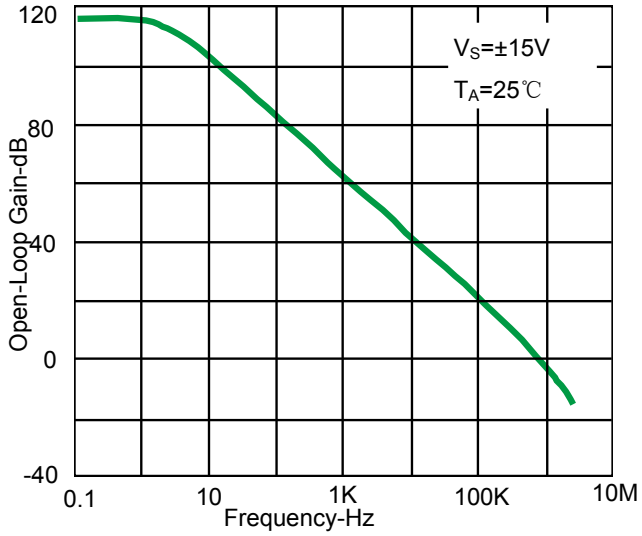


Figure 16.Open-Loop Frequency Response

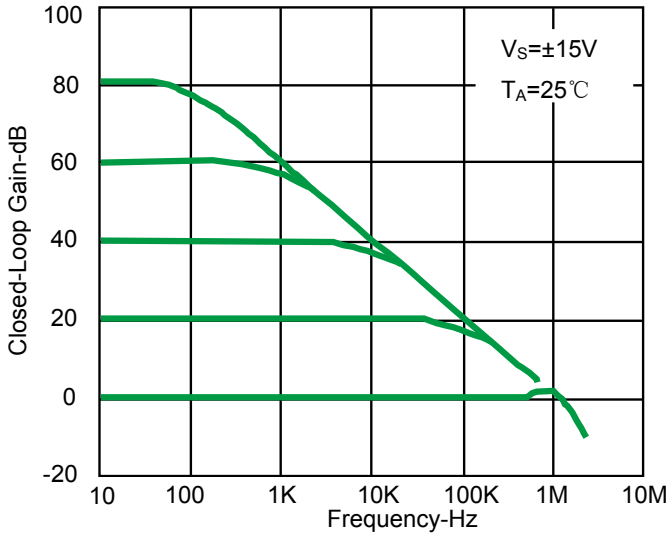


Figure 17.Closed-Loop Response for Various Gain Configurations

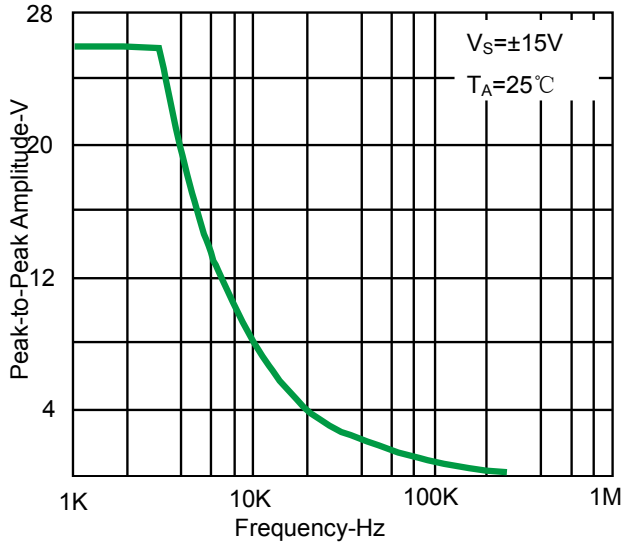


Figure 18. Maximum Output Swing vs. Frequency

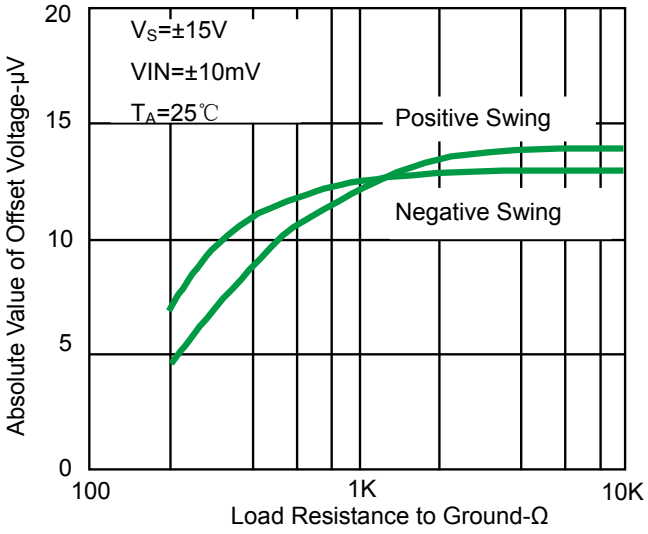


Figure 19. Maximum Output Voltage vs. Load Resistance

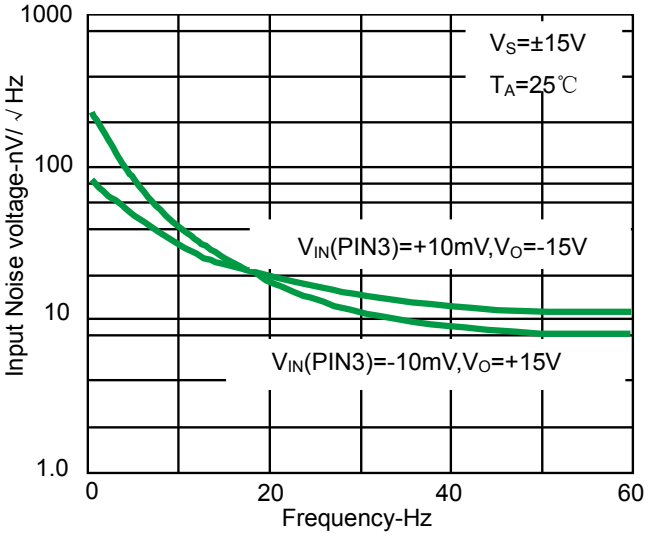


Figure 20. Power Consumption vs. Power Supply

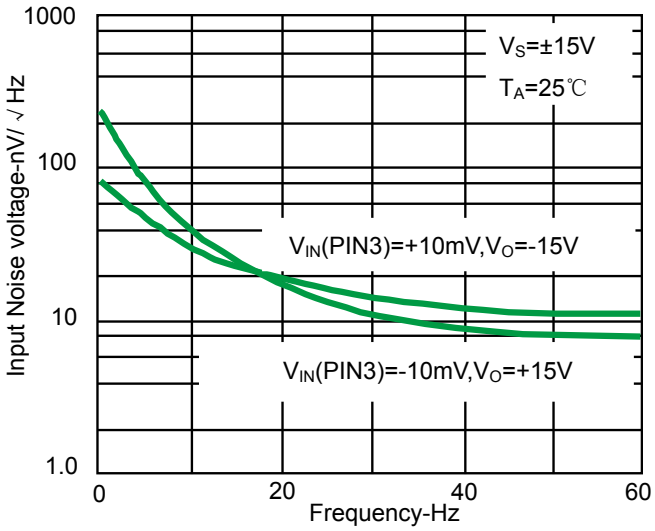


Figure 21. Output Short-Circuit Current vs. Time

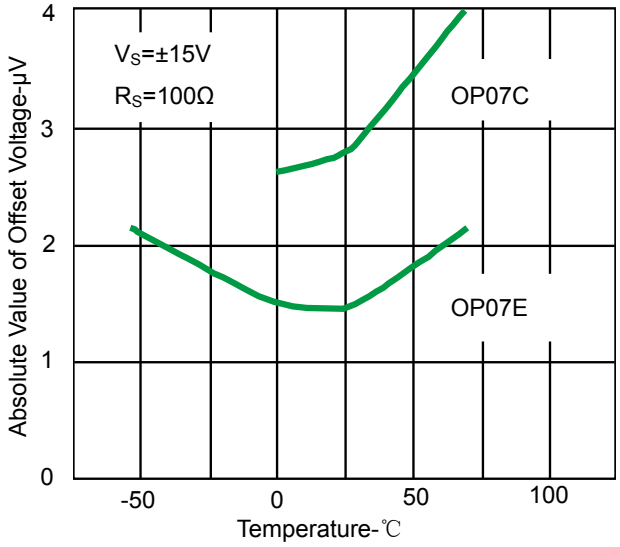


Figure 22 Untrimmed Offset Voltage vs. Temperature

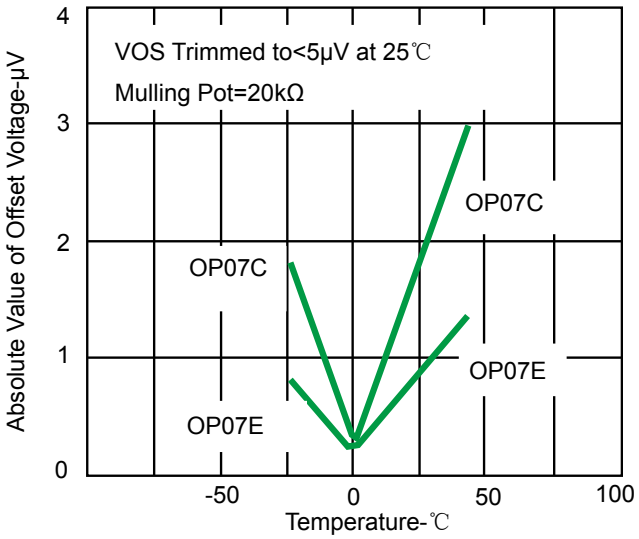


Figure 23. Trimmed Offset Voltage vs. Temperature

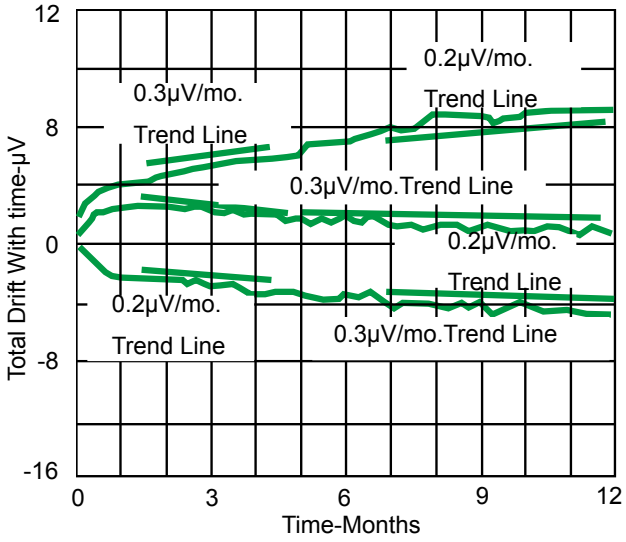


Figure 24. Offset Voltage Stability vs. Time

Typical Applications

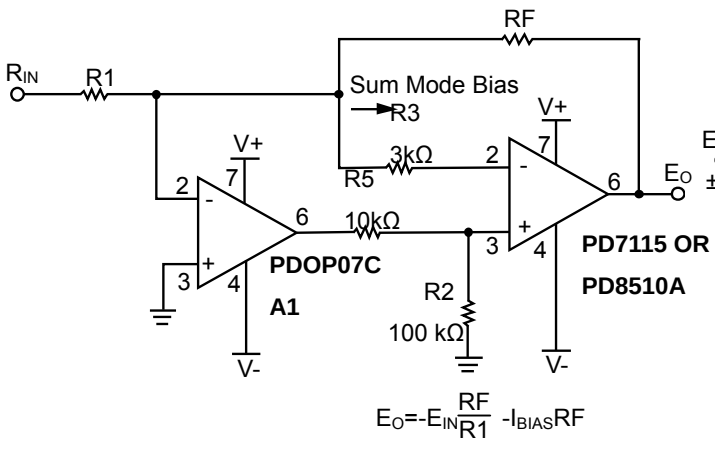


Figure 25. Typical Offset Voltage Test Circuit

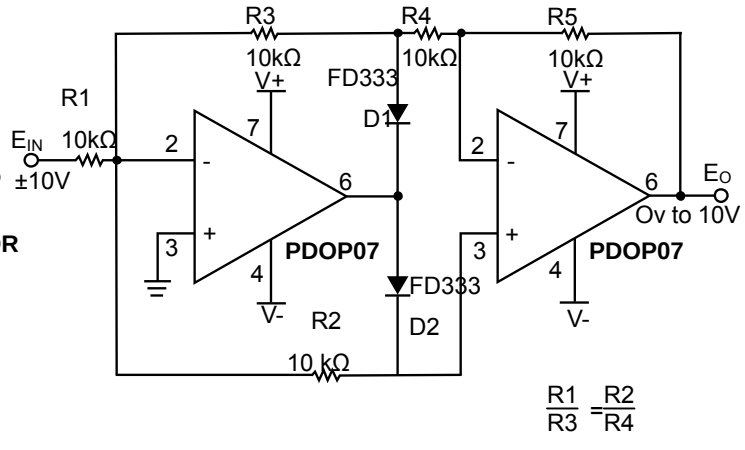


Figure 26. Burn-In Circuit

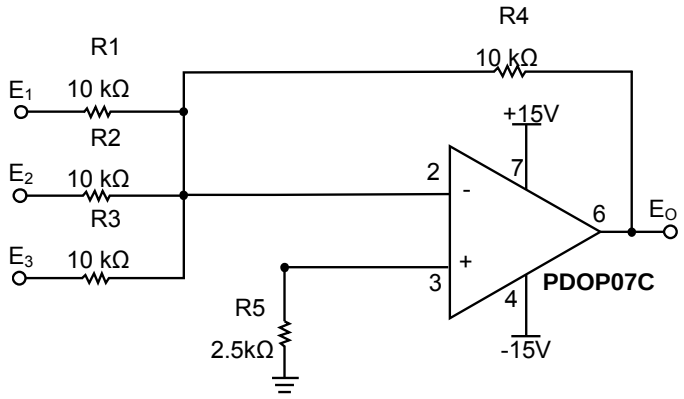
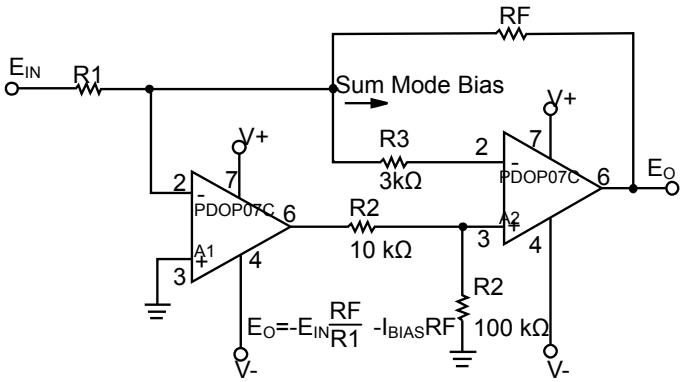


Figure 27. Typical Low-Frequency Noise Circuit



Pin outs Shown for J,P, and Z Packages

Figure 28. High-Speed, Low VOS Composite Amplifier

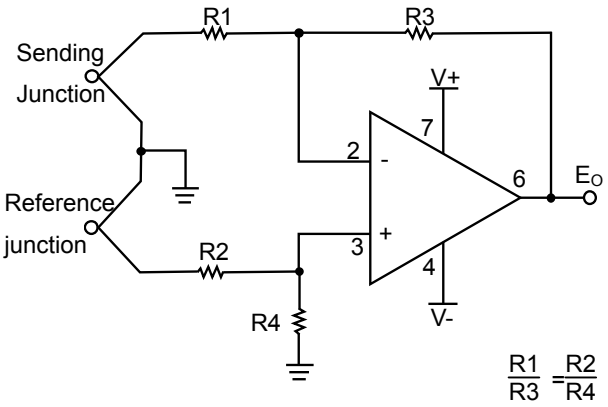
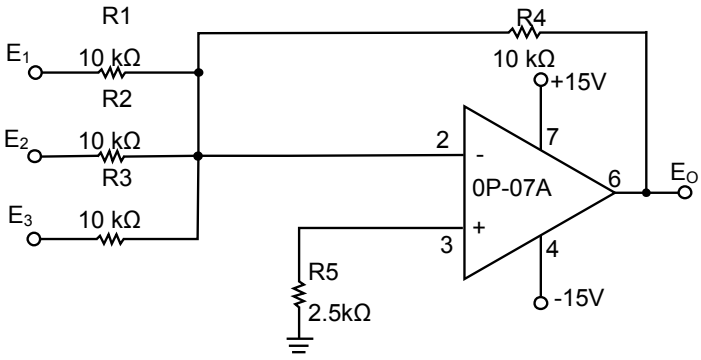


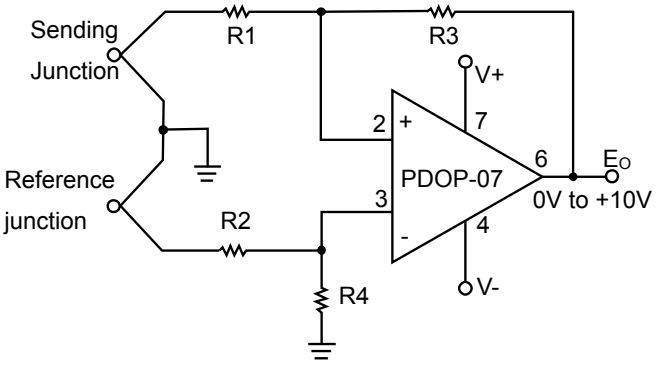
Figure 29.Optional Offset Mulling Circuit



Pin outs Shown for J,P, and Z Packages

Figure 30. Adjustment-Free Precision Summing Amplifier

Typical Applications



Pin outs shown for J,P, and Z Packages

Figure 31. High-Stability Thermocouple Amplifier

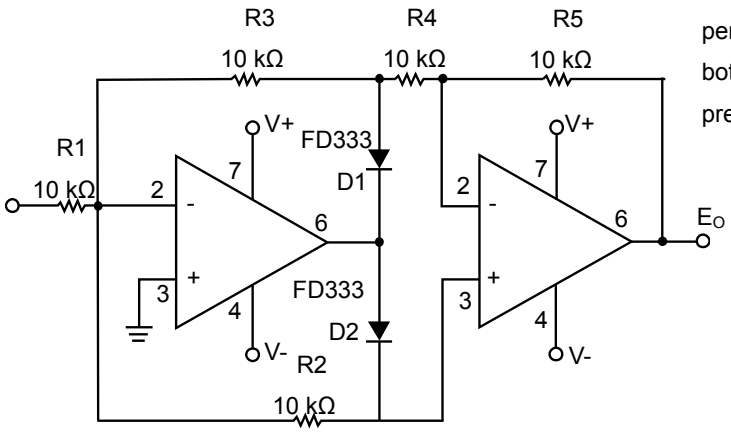
Applications Information

PDOP07 series units may be substituted directly into 725, 108A/308A* and PDOP05 sockets with or without removal of external compensation or nulling components. Additionally, the PDOP07 May be used in unnulled 741 type sockets. However, if conventional 741 nulling circuitry is in use,it should be modified or removed to enable proper PDOP07 operation. PDOP07 offset voltage may be nulled to zero through use of a potentiometer (see offset nulling circuit diagram).

Precision Absolute-Value Circuit

The PDOP07 provides stable operation with load capacitance of up to 500 pF and ±10V swings; larger capacitances should be decoupled with a 50 Q decoupling resistor

Stray thermoelectric voltages generated by dissimilar metals

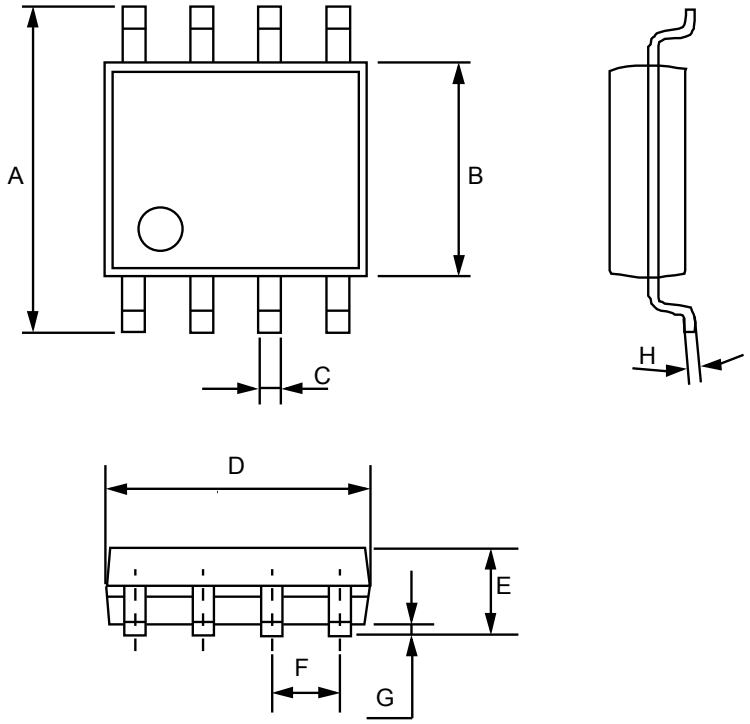


Pin outs Shown for J,P, and Z Packages

Figure 32. Precision Absolute-Value Circuit

at the contacts to the input terminals can degrade drift performance. Therefore, best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

Product dimension (SOIC-8)



Dim	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	5.800	6.200	0.228	0.244
B	3.800	4.000	0.150	0.157
C	0.330	0.510	0.013	0.020
D	4.700	5.100	0.185	0.200
E	1.350	1.750	0.053	0.069
F	1.270（BSC）		0.050（BSC）	
G	0.100	0.250	0.004	0.010
H	0.170	0.250	0.006	0.010

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